What is claimed is:

1. A semiconductor integrated circuit device comprising:

an analog signal generating section for outputting an analog signal; and

a predetermined signal storing section for storing at least one predetermined signal that is supplied to the analog signal generating section and sets the analog signal to a predetermined value,

wherein digital signals are used for input/output interface to external terminals,

for adjusting the analog signal, the semiconductor integrated circuit device further comprises a judgment section for outputting at least one judgment signal that corresponds to a comparison result of the analog signal corresponding to at least one adjustment signal and the predetermined value generated based on power source voltage, for each adjustment signal supplied to the analog signal generating section in accordance with a test signal, and

in case the judgment signal judges that the analog signal has the predetermined value, the adjustment signal corresponding to the as-judged analog signal is stored in the predetermined signal storing section as the predetermined signal.

2. A semiconductor integrated circuit device according to claim 1 further comprising a signal selecting section that is controlled by the test signal and supplies either the adjustment signal or the predetermined signal to the analog signal generating section.

3. A semiconductor integrated circuit device according to claim

1, wherein the adjustment or the predetermined signal is digital signals of two or more than two bits and inputted to a decoding section arranged at a preceding stage of the analog signal generating section.

4. A semiconductor integrated circuit device according to claim 1, wherein the predetermined value is a predetermined analog value region between a first comparison reference value and a second comparison reference value, and the judgment signal judges which analog value region sectioned by two or more comparison reference values including the first and the second comparison reference values the analog signal exists in.

5. A semiconductor integrated circuit device according to claim 4, wherein the judgment section includes:

a plurality of comparing sections for comparing the analog signal with each of the two or more comparison reference values; and

an encoding section for outputting encoding signals in a manner of receiving output signals from the plurality of comparing sections and discriminating the analog value region where the analog signal exists.

6. A semiconductor integrated circuit device according to claim 4, wherein the two or more comparison reference values are obtained by lowering/dividing power source voltage.

7. A semiconductor integrated circuit device according to claim 1, wherein the analog signal generating section is an internal power source voltage generating section and outputs internal

power source voltage as the analog signal.

8. A semiconductor integrated circuit device according to claim 1, wherein the predetermined signal storing section includes memory elements or fuse elements, and the predetermined signal storing section is controlled inside the semiconductor integrated circuit device based on the judgment signal for data-write on the memory elements or cutting out the fuse elements.

9. A semiconductor integrated circuit device according to claim 1, wherein the judgment signal is a digital signal and outputted from the external terminal.

10. A semiconductor integrated circuit device according to claim 1, wherein the predetermined signal storing section includes fuse elements or memory elements, and based on external control to the judgment signal outputted, data-write on the memory elements or cutting out of the fuse elements is conducted.

11. A semiconductor integrated circuit device according to claim 1 further comprising an adjustment signal generating section for outputting the adjustment signal in order under activation control by the test signal.

12. A semiconductor integrated circuit device according to claim 11, wherein the adjustment signal generating section includes an oscillation section for outputting an oscillation signal having predetermined frequency, and counter section for counting the oscillation signal, transitioning and outputting the adjustment signal with constant cycle based on the predetermined frequency.

13. A semiconductor integrated circuit device according to claim 1 further comprising a self-diagnosis test circuit for executing predetermined tests for the predetermined internal circuits inside the semiconductor integrated circuit device, wherein adjustment test of the analog signal is executed as one of tests by the self-diagnosis test circuits.

14. A semiconductor integrated circuit device according to claim 13, wherein the test signal, the adjustment signal, and the judgment signal are inputted to/outputted from the self-diagnosis test circuit.

15. A semiconductor integrated circuit device comprising:

an analog signal generating section for outputting an analog signal; and

a predetermined signal storing section for storing at least one predetermined signal that is supplied to the analog signal generating section and sets the analog signal to a predetermined value,

wherein digital signals are used for input/output interface to external terminals, and the semiconductor integrated circuit device further comprises virtual load section for varying load against the analog signal in response to a load setting signal to be supplied.

16. A semiconductor integrated circuit device according to claim 15, wherein the analog signal generating section is an internal power source voltage generating section and outputs internal power source voltage as the analog signal, and the load is a

current source circuit for generating load current.

17. An adjustment method of a semiconductor integrated circuit device that generates an analog signal having a predetermined value based on at least one predetermined signal stored and uses digital signals for input/output interface to external terminals, for adjusting the analog signal, the adjustment method comprising the steps of:

a signal generating step for generating the analog signal that corresponds to at least one adjustment signal;

a judgment step for judging a comparison result of the analog signal generated and the predetermined value generated based on power source voltage, the judgment step being executed inside the semiconductor integrated circuit device; and

a storing step for storing the adjustment signal as the predetermined signal in case the analog signal is judged as having the predetermined value through the judgment step.

18. An adjustment method of a semiconductor integrated circuit device according to claim 17, wherein the adjustment signal makes stepwise transition and the signal generating step and the judgment step are repeated for each adjustment signal.

19. An adjustment method of a semiconductor integrated circuit device according to claim 17, wherein the storing step is executed inside the semiconductor integrated circuit device.

20. An adjustment method of a semiconductor integrated circuit device according to claim 17, wherein judgment of the comparison result is outputted from at least one of the external terminals

in a form of at least one digital signal.

21. An adjustment method of a semiconductor integrated circuit device according to claim 20, wherein the storing step is controlled outside the semiconductor integrated circuit device.

22. An adjustment method of a semiconductor integrated circuit device according to claim 21, wherein the storing step includes: a signal obtaining step for obtaining the adjustment signal as the predetermined signal in case the analog signal is judged as having the predetermined value; and a write step for writing the obtained predetermined signal in a predetermined signal storing section.

23. An adjustment method of a semiconductor integrated circuit device that generates an analog signal having a predetermined value based on at least one predetermined signal stored and uses digital signals for input/output interface to external terminals, the adjustment method adjusting the analog signal through a virtual load step for varying load against the analog signal in accordance with a load setting signal.